CMOS Integration of Area-dependent PCMO-based ReRAM-Devices

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Resistive Random Access Memory (RRAM) is a promising technology for next-generation non-volatile memory and neuromorphic computing due to its simple structure, fast switching, and compatibility with back-end-of-line (BEOL) integration [1]. In this work, we focus on the chip-level integration of non-filamentary RRAM devices based on $Pr_xCa_{1-x}MnO_3$ (PCMO) combined with a tunnel oxide layer. Unlike conventional filamentary transition metal oxide devices, this heterostructure exhibits area-dependent resistive switching [2], enabling stable intermediate resistance states suitable for analog neuromorphic applications [3]. Furthermore, the device current of area dependent devices can be effectively tuned by adjusting the electrode area, offering enhanced design flexibility and enabling low-power operation in miniaturized devices. [4] These characteristics position the device concept as a strong candidate for energy-efficient neuromorphic computing hardware.

However, the area dependence also presents a limitation. In particular, the strong area dependence leads to increased resistance for smaller device dimensions, which can limit reliable current readout. To address this, the substrate temperature during the large area pulsed laser deposition (LAPLD) of PCMO was elevated to 400°C to reduce the resistance for downsized devices, while maintaining CMOS compatibility. This approach enables improved device performance at reduced feature sizes and supports scalable integration.

To fully exploit these device-level advantages in practical applications, crossbar structures of area-dependent PCMO/WO_x RRAM devices were successfully integrated into a commercially available 180 nm silicon CMOS chip, demonstrating compatibility with back-end-of-line (BEOL) integration requirements. Overall, the demonstrated device concept and integration strategy ensures circuit compatibility, and manufacturability at the system-level, which highlights the potential of PCMO-based RRAM for energy-efficient hardware implementations.

Single devices and 1T1R structures were systematically characterized using DC and pulsed measurements to study the SET, and RESET behavior, endurance, and retention. The results demonstrate reliable resistive switching. Retention measurements on devices with electrode variations indicate an optimization of the resistance states with Ta as the electrode material, suggesting non-volatile behavior suitable for in-memory computing.

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