Improving RRAM Test Efficiency and Reliability Through Combined DfT and Temperature-Aware Strategies

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This work addresses the challenge of reliability evaluation and test efficiency in resistive RAM (RRAM) technologies by combining Design-for-Testability (DfT) techniques, aging modeling, and temperature-assisted fault analysis.

First, a DfT-based strategy is proposed to enable both manufacturing testing and online monitoring of RRAM cells during lifetime [1]. The approach extends conventional manufacturing-oriented circuitry by incorporating an aging-aware functionality capable of identifying fault-free cells at time zero and detecting degradation during operation. Figure 1 illustrates the architecture of the proposed strategy. The method is validated using a 4×4 word-based RRAM array implemented in a 28nm TSMC technology, demonstrating effective detection of resistance deviations associated with both defects and aging. Although the proposed solution introduces an area overhead of approximately 2.75× compared to sense amplifiers, this overhead can be reduced through optimized design granularity.

To further support reliability analysis, an aging model based on write operations is introduced for bipolar filamentary VCM-based 1T1R ReRAM cells. The model establishes a relationship between the number of programming cycles and the oxygen vacancy (Vo) concentration, enabling the characterization of endurance degradation over time. Different aging behaviors are explored by varying the minimum Vo level, and the degradation trend is captured using a polynomial function. A case study also implemented in 28nm CMOS technology with the JART VCM compact model demonstrates that the proposed model accurately predicts device degradation, including RESET-related failures, while enabling efficient circuit-level simulations.

Finally, temperature is investigated as a stress condition to facilitate fault propagation and reduce test time [2]. A 3×3 word-based RRAM array implemented with a 130nm PTM technology is used to evaluate multiple defect scenarios under different temperature conditions (−40°C, 25°C, and 100°C). The results show that temperature significantly impacts the observability of both conventional and parametric faults, with some defects becoming detectable only within specific thermal ranges. These findings highlight the importance of temperature-aware testing strategies.

Overall, the combination of DfT-based monitoring, physics-aware aging modeling, and temperature-assisted testing provides a comprehensive framework to improve fault detection, reduce test time, and the detection of aging effects during operation in emerging RRAM technologies.

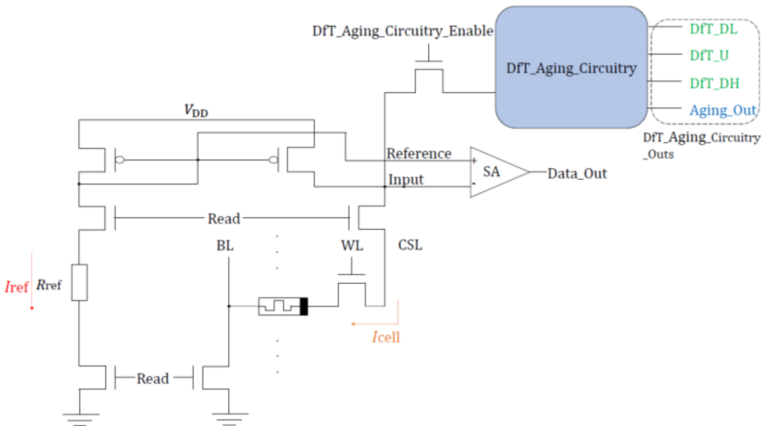

Figure 1: Architecture of the proposed strategy including the DfT Aging Circuitry.

[1] Copetti et al., IEEE Latin American Test Symposium, 26, 1–6, 2025.

[2] Copetti et al., Microelectron. Reliab., 175, 115919, 2025.