Electrochemical random-access memory devices for neuromorphic computing

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The rise of artificial intelligence (AI) is driving an unprecedented increase in the energy consumption of information technology infrastructures, such as data centers. The physical separation between computing and memory units in traditional digital computing systems leads to poor energy efficiency and latency due to data shuttling in the bus. These trends call for novel computing paradigms, such as the in-memory computing (IMC) concept, in which highly specialized computing tasks are executed in parallel within memory arrays.

Electrochemical random-access memories (ECRAM) are three terminal resistive memory devices, which appear as promising devices for IMC, due to several figures of merit such as: low power operation, highly precise electrical control, low variability, back-end-of-line compatibility with CMOS and 3D-integration.

Our aim is to deepen the understanding of the physical mechanisms underlying ECRAM operation, an aspect that remains highly debated but is crucial for developing next-generation devices. We fabricated ECRAM devices by e-beam evaporation and lift-off techniques with different geometries (channel length and width in the 5 to 20 µm range) and conducted a thorough study of the materials and post-deposition thermal treatments to tune the WO_3 channel and gate stack electrical properties. Fig.1a shows the cross-sectional sketch of an ECRAM device; it comprises metallic drain-source and gate terminals (W), a metal-oxide channel and reservoir (WO_3), and an electrolyte layer (HfO_2). Physical and chemical characterization techniques, including XPS, AFM, and ellipsometry, were used to study the material stack. The functionality of the fabricated ECRAMs was assessed by electrical characterization, according to the scheme in Fig. 1a. The application of a voltage to the gate terminal allows the modulation of channel resistance, measured through the drain-source terminals. Fig. 1b shows a representative curve of the current in the channel (I_{DS}) probed at 100 mV as a function of a voltage ramp applied to the gate; I_{DS} displays a counterclockwise hysteresis of several orders of magnitude. Fig. 1c shows the corresponding measured gate current (I_{GS}) which is ascribed to the movement of ions from the reservoir into the channel. The device performance was evaluated in terms of channel length, memory window, and retention.

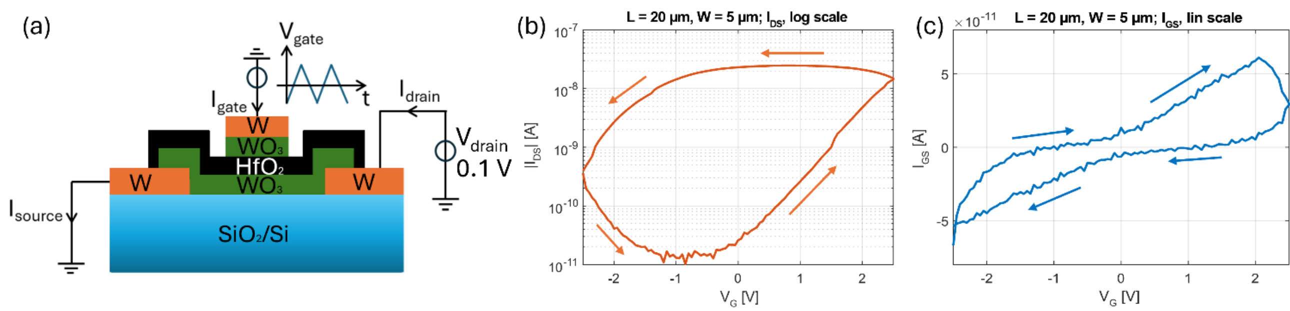

Figure 1: a) Schematic cross-sectional representation of the ECRAM. b) Channel current probed at a V_{DS} of 0.1 V as a function of sweeping gate voltage. c) Measured gate current.