3D integration of next generation electronic devices in the back-end-of-the-line

Sebastian Oschmann(1), Lukas Völkel(1), Florian Brehmer(2), Shubhada Sunil Shetti(2), Thomas Mikolajick(2, 3), Max Lemme(1,4)

(1) Chair of Electronic Devices, RWTH Aachen University, Otto-Blumenthal-Str. 25, 52074 Aachen, Germany.
(2) Chair of Nanoelectronic Materials, TU Dresden, Nöthnitzer Str. 64, 01187 Dresden, Germany.
(3) NaMLab gGmbH, Nöthnitzer Str. 64 a, 01187 Dresden, Germany.
(4) AMO GmbH, Advanced Microelectronic Center Aachen, Otto-Blumenthal-Str. 25, 52074 Aachen, Germany.

The semiconductor industry has traditionally focused on scaling transistors to increase the number of components per integrated circuit to keep up with Moore's law [1]. However, since the beginning of the 21st century, down scaling transistor size has become extremely difficult. The TRR Active-3D project aims to establish a new approach for microelectronic systems by integrating different devices in the back-end-of-the-line (BEOL) using 3D architectures and hence, moves beyond conventional planar scaling. This novel circuit arrangement can enhance functionality, device density and energy efficiency [2]. While the sub-projects focus on single device concepts and their circuit-level implementation, Project C01 addresses reliable interconnection, co-fabrication and standardization across the involved research sites.

One main challenge is the realization of advanced interconnecting metallization schemes of linking diverse devices with different materials, geometries and electrical requirements. Aiming this, the project explores hybrid metallization strategies, local contact materials and atomic layer deposition (ALD) processes for conformal and precise fabrication. Additional challenges include multi-directional contacting (top, bottom and lateral), integration of vertical and lateral device architectures and the development of standardized fabrication, characterization and data protocols. Harmonizing these processes across sites ensures reproducibility, efficient sample exchange, and scalable co-integration.

The project is relevant for neuromorphic computing, where dense integration of memory and logic, high connectivity and energy efficiency are essential. The 3D BEOL integration approach enables tight coupling of memory elements (e.g. resistive switching devices) and logic devices (e.g. field-effect transistors), supporting in-memory and brain-inspired computing architectures [3]. By reducing data movement and enabling compact, highly interconnected structures, Active-3D provides a promising hardware platform for energy-efficient neuromorphic systems [4].

[1] K. S. Kim et al., Nat. Nano., **19**, 895-906, 2024.

[2] H. Kim et al., Nat. Rev. Electr. Eng., **2**, 835-845, 2025.

[3] S. Ju Kim et al., 2D Mater. and Appl., **8,** 70, 2024.

[4] H. An et al., VLSI Journ., **65,** 273-281, 2019.