Hardware Realization of Photonic Neuromorphic Reservoir Computing for Optical Network Monitoring and Beyond

Enes Şeker(1,2), Mahdi Kaveh(3), Rijil Thomas(1), Rahul Garg(1), Jonathan Lahey(1), Shi Li(6), Guillermo von Hünefeld(3,4), Stephan Suckow(1), Vinay Singh(6), Joseph Hopfmüller(5), David Stahl(5), Colja Schubert(3), Ronald Freund(3,4), and Max C. Lemme(1,2)

(1) AMO GmbH, Otto-Blumenthal-Straβe 25, 52074 Aachen, Germany

(2) RWTH Aachen University, Chair of Electronic Devices, Otto-Blumenthal-Straße 25, 52074 Aachen, Germany

(3) Fraunhofer Institut für Nachrichtentechnik, Heinrich Hertz Institute (HHI), Einsteinufer 37, 10587 Berlin, Germany

(4) Technical University of Berlin, Photonic Communication Systems, Straße des 17. Juni 135, 10623 Berlin, Germany

(5) ID Photonics GmbH, Anton Bruckner Straße 6, 85579 Neubiberg, Germany

(6) VPIphotonics GmbH, Hallerstraße 6, 10587, Berlin, Germany

seker@amo.de

Photonic reservoir computing (PRC) is an emerging neuromorphic paradigm that exploits passive integrated photonic circuits, enabling complex temporal data processing without the energy cost of fully digital neural networks [1,2]. We previously demonstrated a neuromorphic photonic integrated circuit (NeuroPIC) on a silicon-on-insulator (SOI) platform achieving up to 100% accuracy in modulation format identification (MFI) of telecom C-band QAM signals at 32 GBaud [3,4]. We now extend the NeuroPIC platform to silicon nitride (SiN), a lower-loss material that enables reduced signal attenuation in the reservoir circuit. We extend the application from MFI to the more demanding task of channel equalization, requiring symbol-by-symbol compensation of the fiber effects.

A key finding from our earlier work on 1st generation NeuroPIC was that variations in the reservoir internode delays change its output in such a way that it could improve the final performance. Motivated by this, we conducted a simulation study comparing reservoir configurations for the channel equalization task on 32 Gbaud 16-QAM signals over a 10 km standard single-mode fiber link. Our 1st generation NeuroPIC uses internode delay lines of 1.5 symbol duration (~47 ps), optimised for the MFI task. However, channel equalization requires compensation of inter-symbol interference on the timescale of adjacent symbols, suggesting that much shorter delay lines are required. We implemented two independent variations: 1) shortening the delay lines to 0.1 symbol durations (~3 ps); 2) replacing the planar 4-port node connectivity architecture with a non-planar topology, with the intention to increase the diversity of interference paths inside the reservoir.

Simulation results reveal that delay line length is a dominant factor for equalization performance. Using 1.5 symbol duration internode delays, both the planar 4-port and the non-planar architecture achieve only marginal bit error ratio (BER) improvement by a factor of ~2 over the distorted signal BER of $\sim 4.75 \times 10^{-2}$, indicating that this configuration is not suitable for the equalization task. Switching to 0.1 symbol duration delay lines dramatically improves performance. The planar 4-port design achieves an improvement by a factor of ~61, while the non-planar architecture achieves an improvement of ~85.

In conclusion, we present a simulation study of SiN based PRC for optical channel equalization, identifying sub-symbol duration internode delays as a critical design parameter and the non-planar reservoir topology as a further performance enhancer.

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