LOKI: a 0.266 pJ/SOP Digital SNN Accelerator with Multi-Cycle Clock-Gated SRAM in 22nm

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Bio-inspired sensors like Dynamic Vision Sensors (DVS) and silicon cochleas are often combined with Spiking Neural Networks (SNNs), enabling efficient, event-driven processing similar to biological sensory systems. To realize the low-power constraints of the edge, the SNN should run on a hardware architecture that can exploit the sparse nature of the spikes. In this work, we show LOKI (Figure 1), a digital architecture for Fully-Connected (FC) SNNs. By using Multi-Cycle Clock-Gated (MCCG) SRAMs, LOKI can operate at 0.59 V, while running at a clock frequency of 667 MHz. At full throughput, LOKI only consumes 0.266 pJ/SOP. We evaluate LOKI on both the Neuromorphic MNIST (N-MNIST) and the Keyword Spotting (KWS) tasks, achieving 98.0% accuracy at 119.8 nJ/inference and 93.0% accuracy at 546.5 nJ/inference respectively.

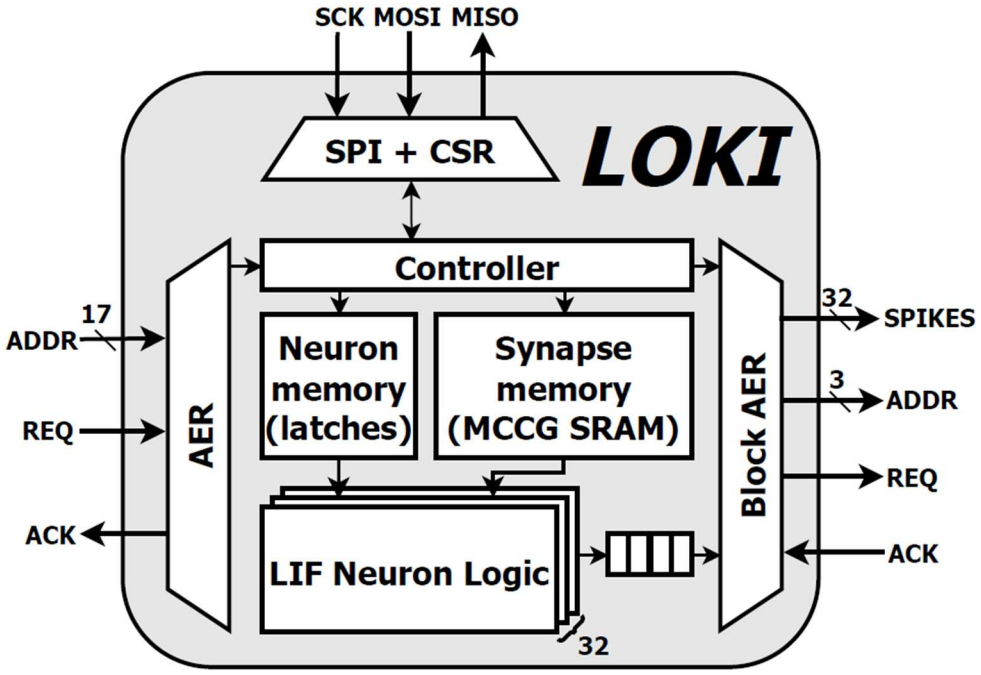

Figure 1: **Block diagram of the LOKI digital SNN accelerator.** Spikes are received through the AER interface, while parameters are programmed through the SPI interface. Membrane potentials are updated by the LIF Neuron Logic. Output spikes are sent out through the block AER.