CMOS-Integrated Nanoscale MoS_2 Memristors with Low-Voltage Operation

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Layered two-dimensional materials (2DMs) such as hexagonal boron nitride (h-BN) and molybdenum disulfide (MoS_2) have been widely explored as resistive switching (RS) media for nonvolatile memories, electronic switches, and neuromorphic computing applications [1,2]. 2DM-based memristors exhibit ultra-low energy consumption, high ON/OFF ratios, and stable switching at sub-nanometer thicknesses [3-8].

Recently, h-BN memristors have been successfully integrated onto silicon complementary metal–oxide–semiconductor (CMOS) chips. However, their operation requires relatively high voltages (1.5-2 V) [3,4]. In contrast, MoS_2 memristors have shown lower operating voltages [6-8], making them suitable for low-power CMOS integration. To date, most reported MoS_2 memristors have been fabricated as standalone devices with active areas exceeding 1 μm^2 on SiO_2/Si substrates [6-8], limiting scalability and practical implementation in advanced semiconductor technology.

Here, we demonstrate the first integration of nanoscale (~0.015 μm^2) MoS_2 memristors on silicon CMOS microchips fabricated in a 350 nm technology node (Figure 1) [9]. The Au/Ag/MoS_2/Pd memristors are integrated on the fourth metal layer (M4), where Pt/Ta pads connect the third metal layer (M3) of the back-end-of-line (BEOL) interconnections to CMOS transistors, forming one-transistor-one-resistor (1T1R) cells. These cells exhibit forming-free, nonvolatile RS with ultra-low operating voltages (~0.23 V for the SET and ~–0.1 V for the RESET) and high reproducibility across multiple cycles and devices. RS is based on the electrochemical metallization (ECM) mechanism, in an applied electric field drives the migration of Ag ions from the active electrode through the MoS_2 layer to the inert counter electrode, forming and rupturing metallic conductive filaments. These results represent a significant step toward CMOS-compatible 2DM-based memristive technologies.

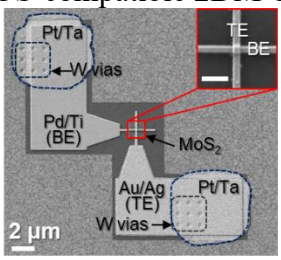

Figure 1: Top-view scanning electron microscopy image of a fabricated Au/Ag/MoS_2/Pd memristor integrated with pre-patterned Pt/Ta pads through W vias. The inset presents a magnified image of the intersection between the top and bottom electrodes, which defines an active area of approximately 0.015 μm^2. Inset scale bar: 500 nm.

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