Sub-Nanosecond SET and RESET Switching Dynamics in SnTe-Doped In_3SbTe_2 Phase-Change Memory

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Phase-change memory (PCM) devices are promising candidates for next-generation non-volatile memory and neuromorphic computing, owing to the large resistance contrast between their amorphous and crystalline phases [1]. This contrast enables analog conductance modulation and multi-level storage, making PCM attractive for in-memory computing and artificial synaptic applications. Despite extensive research, switching dynamics in the sub-nanosecond regime remain insufficiently understood, as most studies have focused on nanosecond or longer timescales where intermediate crystallization dynamics, which govern variability and reproducibility [3, 4], are difficult to access experimentally [1, 2].

This work presents a systematic experimental investigation of SET and RESET switching kinetics in SnTe-doped In_3SbTe_2 (SIST) PCM devices using a dedicated RF measurement setup capable of applying electrical pulses down to the sub-nanosecond timescale. To investigate the SET switching behavior, pulse amplitude and duration were systematically varied from 2 ns to 100 ns. The resulting resistance heatmaps (Fig. (a)) revealed two distinct switching regimes, separated by a non-switching intermediate region attributed to resistance drift and structural relaxation. The low-voltage regime exhibits pronounced cycle-to-cycle variability, consistent with stochastic nucleation-dominated crystallization, while the high-voltage regime shows deterministic and reproducible switching, characteristic of growth-dominated crystallization, with this distinction demonstrated consistently across multiple devices.

RESET switching kinetics were investigated in 40% SIST devices using pulse widths ranging from 50 ps to 250 ps at three different voltage amplitudes. The results revealed a clear dependence of the amorphization kinetics on both pulse amplitude and duration, as shown in Figure (b). At higher voltages, reliable amorphization was achieved at pulse widths below 100 ps, which is faster than the 200 ps RESET switching previously reported for GST-based PCM cells [5]. R_{HRS}/R_{init} ratios exceeding 10^3 confirm that RESET switching is governed by a thermally driven melt-quench mechanism [1], where higher voltages enable faster amorphization at shorter pulse widths.

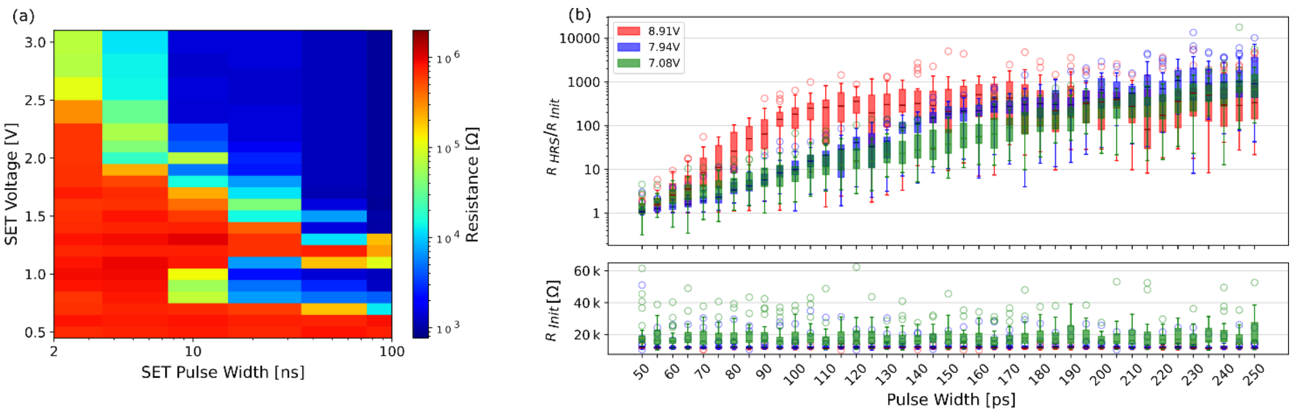

Figure: (a) Heatmap of SET switching kinetics in a 10% SIST device revealing distinct nucleation-dominated and growth-dominated crystallization regimes. (b) RESET switching kinetics of a 40% SIST device at three voltages.

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