Design of Multi-Encoded Leaky-Integrate-and-Fire Neuron in 28 nm CMOS

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Designing a neural encoder that can translate signals into spikes is essential for applying input to spiking neuromorphic systems. Each encoding scheme has its own advantages, but the most suitable one depends on architectural constraints and application requirements. Ultra-low-latency edge inference favours temporal time-to-first-spike (TTFS), temporally sensitive signal processing benefits from inter-spike-interval (ISI) encoding precision, and large-scale noise-tolerant systems may prefer rate coding. Most reported CMOS neuron circuits in Table I are optimised for a single encoding paradigm, limiting adaptability across diverse applications. The most suitable encoding scheme depends on the application, architecture, and requirements of the system. In this work, we present a compact CMOS circuit of a multi-encoded leaky-integrate-and-fire (MELIF) neuron capable of translating the input sensory data into rate-encoded and temporal TTFS-encoded signal. The MELIF neuron exhibiting TTFS encoding is further extended to demonstrate inter-spike-interval (ISI) encoding. In addition to its multi-encoding property, the neuron circuit offers various adjustable features such as threshold, pulse width and refractory period control which facilitates the use of the proposed neuron for various applications at different frequencies. Simulations of the designed neuron circuit in 28 nm technology verify its multi-encoded property and adjustable features. Table I compares the state-of-the-art works related to neuron circuit design. The energy/spike of the proposed MELIF neuron is comparable to other works with least no. of transistors. Also, the proposed neuron exhibits various tunable features such as controllable refractory period, pulse width and threshold. Although work [5], has shown multiple encodings, however, the circuit required in rate encoding was different from TTFS encoding. In particular, the MELIF neuron is the only neuron that can exhibit multiple encoding within the same circuit by changing the control voltages.

Table 1: Comparison of CMOS neurons circuit design in various State-of-the-art works.

	Technology (nm)	Supply Voltage	Refractory Period Control	Pulse width Control	Threshold Control	Encoding Type	Multi-Encoding in same circuit	Transistors/Capacitors	Area (μm^2)	Energy/ spike
This Work	28	0.6 V	Yes	Yes	Yes	Rate, TTFS, ISI	Yes	9/2	225	0.7 pJ
TCAS II 2024[1]	65	0.5 V	Yes	No	No	Rate	No	27/3	2035	3.6 pJ
TVLSI 2024[2]	90	1.3 V	No	No	No	TTFS	No	23/2	-	4.74 pJ
TNANO 2025[3]	180	1 V	No	No	No	Rate	No	20/1	2412	1.2 pJ
TVLSI 2023[4]	180	1.8 V	Yes	No	No	TTFS, ISI	No	12/1	924	9.5 pJ
TCAS I 2021[5]	22	0.8 V	Yes	No	No	Rate	No	49/3	900	14 pJ
AICAS 2020[6]	28	1.8 V	No	No	No	rate	No	$>$ 17 + counters + flipflops	-	3.72 nJ

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[6] L. A. Camuñas-Mesa et al., IEEE AICAS, pp. 94-98,2020.