DARWIN: Hardware Efficient Analog In-Memory Computing Using Dendritic ARborized Weights In Neural Networks

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In-memory computing (IMC) with memristive crossbar arrays offers a promising solution to the energy and latency limitations of conventional von Neumann architectures. However, most existing IMC systems rely on perceptron-based neurons, limiting computational flexibility and requiring large, dense networks to achieve competitive performance. Inspired by the nonlinear processing of biological dendrites [1], this work introduces a hardware-efficient IMC architecture, ”DARWIN” [2], that integrates nonvolatile memristive devices as synaptic weights arranged as a tree with volatile memristive devices functioning as integration filters. To further optimize hardware utilization, we incorporate learnable sparsity, enabling the network to automatically discover a compact synaptic pattern within a dendritic tree tailored to the underlying device characteristics. Experimental results demonstrate that the proposed architecture achieves more than two orders of magnitude lower memory footprint and at least an order of magnitude lower power consumption than other in-memory computing architectures. These findings highlight the potential of combining dendritic computation, heterogeneous memristive technologies, and sparsity-aware learning to advance scalable and bio-inspired in-memory computing hardware.

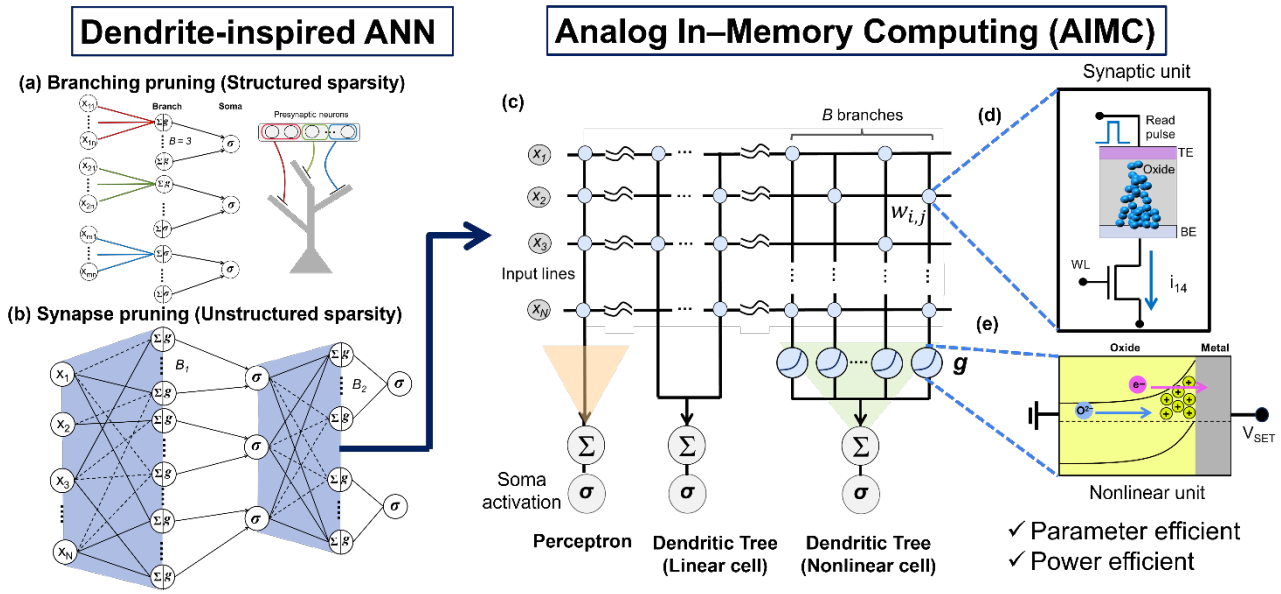

Figure 1: Mapping dendrite-inspired artificial neural networks onto analog in-memory computing (AIMC) substrates. Parameter efficiency in dendritic-tree architectures is achieved through structured sparsity (a) or unstructured sparsity (b). (c, d, e) Schematic illustration of neuron types implemented at memristive crosspoints

[1] Chavlis, S., Poirazi, P. , Nat Commun 16, 943 (2025).

[2] Ming-Jay Yang et al., Neuro Inspired Computational Elements Conference (NICE) (2026)