Mixed-Integer Programming and Simulated Annealing for Placement Optimization of Spiking Neural Networks on a Field-Programmable Spiking Neuron Array

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Mapping spiking neural networks (SNNs) onto circuit-switched neuromorphic inference accelerators such as Field-Programmable Spiking Neuron Arrays (FPSNAs) [1] requires assigning each logical SNN component to a specific hardware resource. As in FPGA design [2], this process has two phases: placement, which maps SNN neurons to hardware neuron sites, and routing, which establishes synapses, the physical interconnects between sites.

The main placement challenge on FPSNAs is minimizing wirelength to improve routability with limited routing resources. SNNs exhibit high fan-out with a strong bias toward local connections - an attribute of biological networks [3] that also appears in layered SNNs and recurrent models (e.g., liquid state machines). These properties clash with common FPGA placement heuristics such as half-perimeter wirelength (HPWL), which assume low-degree nets [4].

We formulate FPSNA placement as a quadratic assignment problem and solve it using two approaches: (1) a mixed-integer linear programming (MILP) reformulation with Kaufman–Broeckx linearization [5] and Gilmore–Lawler bounds [6], and (2) simulated annealing following [7]. We find that on SNNs with small-world connectivity, the MILP yields optimal placements for very small networks (up to 25 neurons) but shows an increasing optimality gap as size grows. Simulated annealing is suboptimal on very small networks yet outperforms MILP beyond 80 neurons and scales to networks of thousands of neurons, aligning with current circuit-switched accelerator capabilities. These results establish a baseline for placement optimization of SNNs on circuit-switched neuromorphic accelerators and improve their deployment flow, contributing to our vision of time-continuous interactions between sensors, emulated SNNs, and actuators.

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