

# Characterization of 1T1R Devices with Different HfO<sub>2</sub>/TiO<sub>x</sub> Stack Modifications

H. Shi<sup>(1)</sup>, O. Artner<sup>(1)</sup>, M. Wierlemann<sup>(1)</sup>, N. Ridder<sup>(1)</sup>, K.-T. Wang<sup>(2)</sup>, Z. Wang<sup>(2)</sup> and S. Hoffmann-Eifert<sup>(1)</sup>

<sup>(1)</sup> Peter-Grünberg-Institut 7, Forschungszentrum Jülich GmbH, <sup>(2)</sup> AMO GmbH

Redox-based Resistive Random-Access Memory (ReRAM) devices are regarded as key building blocks for future neuromorphic computing systems. When combined with a transistor serving as both a selector and a current limiter, 1-Transistor-1-ReRAM (1T1R) arrays can enable in-memory computing operations such as matrix-vector multiplication (MVM).

Conventional front-end-of-line (FEOL) Complementary Metal-Oxide-Semiconductor (CMOS) technology can readily fulfill the transistor requirements of 1T1R devices. However, in the pursuit of sustaining or even surpassing Moore's law, increasing attention has been directed toward the back-end-of-line (BEOL), where BEOL-compatible two-dimensional (2D) material transistors based on transition metal dichalcogenides (TMDs) have emerged as promising candidates for the co-integration of 1T1R architectures.

Among these candidates, MoS<sub>2</sub>-based transistors are particularly attractive for BEOL integration, but their current supply is typically limited to the range of only several to several tens of microamperes [1]. This current limitation imposes stringent requirements on the switching characteristics of the ReRAM cell with HfO<sub>2</sub>/TiO<sub>x</sub> (HOTO) as active switching layer and therefore requires optimization of the HOTO stack [2].

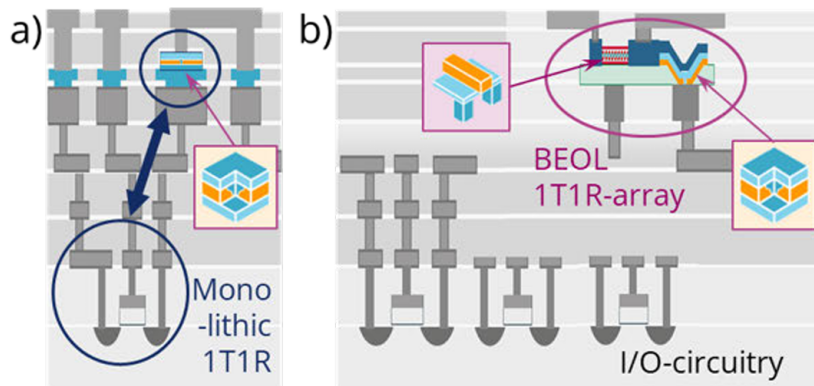


Figure 1: (a) Cross section of a monolithic 1T1R-structure obtained by co-integration of a ReRAM device with a CMOS FEOL transistor. (b) The goal of this project is to realize 1T1R-arrays full-BEOL utilizing a combination of 2D-FETs and ReRAM devices.

In this work, we investigate 1T1R devices co-integrating filamentary Pt/HfO<sub>2</sub>/TiO<sub>x</sub>/Ti ReRAM cells with XFAB 180 nm CMOS technology [3]. By modifying the HOTO active layer stack, we aim to enable reliable forming and resistive switching of the ReRAM cell under reduced current compliance, thereby paving the way for future co-integration with MoS<sub>2</sub>-based field-effect transistors (FETs). This work presents how different HOTO stack configurations affect the electrical characteristics of 1T1R devices and discusses the corresponding electrical measurement results.

[1] A. Piacentini et al., Adv. Electron. Mater., 8 (9), 202200123, 2022.

[2] C. Bengel et al., IEEE Trans. Circuits Syst. I, 67 (12), 4618, 2020.

[3] O. Artner et al., under revision.