Parity Check using In Memory Compute ReRAM macro

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Evaluating Parity Check (PC) equations, the XOR-concatenation of variables, is critical for XOR-satisfiability problems and Low-Density Parity Check (LDPC) decoding. Mobile LDPC applications demand high power efficiency, which traditional Von Neumann architectures struggle to provide due to data movement bottlenecks. In-memory compute (IMC) using ReRAM macros avoids these bottlenecks by performing analog matrix-vector multiplication via Kirchhoff's and Ohm's laws. We previously demonstrated ReRAM's benefits for power efficient and low latency PC evaluation in local search algorithms [1].

Here we compare the previously considered ADC-based IMC approach (*ADC*) against a novel XOR-tree (*XOR*) implementation. In the *XOR* approach, the ReRAM macro provides binary variable assignments to a balanced XOR-tree. In the *ADC* approach, the bitline accumulates an analog sum of assignments, which is digitized. The parity is then extracted from the least significant bit.

Energy statistics were modeled for N variables using capacitance charging for ReRAM, SPICE simulations for 2-input pass-gate XOR trees (22nm node), and survey data for ADCs [3]. Figure 1 shows that the *XOR* approach is optimal by over an order of magnitude in energy per PC evaluation. It also offers lower latency than the *ADC* approach, but has a larger footprint. Furthermore, wordline sharing in parallel PC evaluations makes our estimates a conservative upper bound.

State-of-the-art LDPC ASICs achieve ∼10pJ/bit/iteration [2]. Although this is an upper bound (including message passing), our *XOR*-IMC architecture reaches ∼10fJ/bit/iteration. We conclude that combining IMC with XOR-trees provides at least an order of magnitude energy advantage over the ADC-based IMC and predict a significant energy advantage over traditional ASICs for parity-heavy workloads.

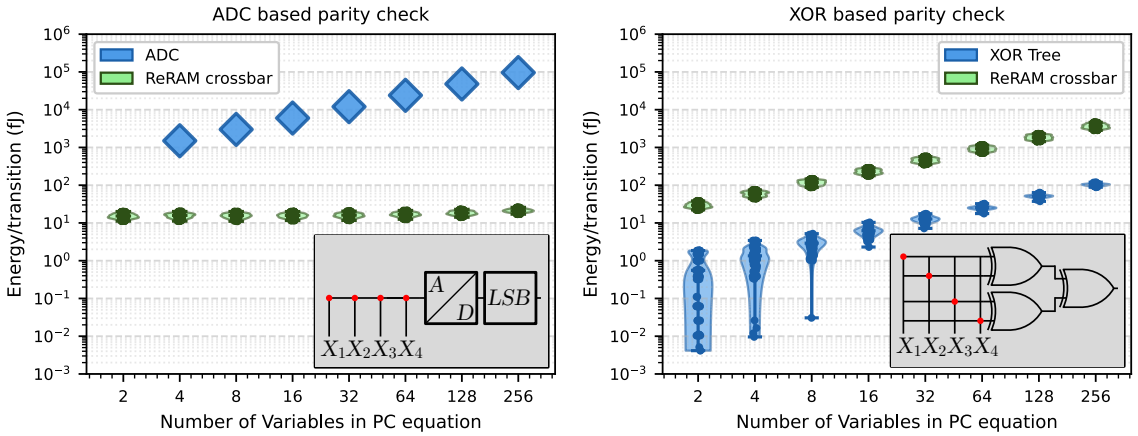

Figure 1: Energy per conversion for *ADC* and *XOR* based IMC parity check evaluation.

[1] H. Im and F. Böhm et al., Nat. Commun., 17, 2026.

[2] M. Li et al., IEEE A-SSCC, 1–5, 2015.

[3] B. Murmann, ADC Performance Survey 1997–2026.