An Ultra-High-Speed Analog MAC for AI Accelerators in Optical Link Equalization

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Driven by the continuous growth of data traffic and the scaling of high-speed optical interconnects, modern optical transmission links operate at increasingly high data rates [1]. At these speeds, channel impairments such as chromatic dispersion, intersymbol interference (ISI), and nonlinear distortion make advanced equalization mandatory [2, 3]. While finite impulse response (FIR)-based equalizers are widely used, their performance becomes limited in these challenging regimes, motivating more powerful machine learning-based approaches, which have been shown to outperform conventional FIR equalizers in optical links [4]. Importantly, both FIR filters and artificial neurons rely on the same core operation: multiply-and-accumulate (MAC).

However, running such algorithms on Digital Signal Processors (DSPs) in real time at multi-Gb/s data rates, together with repeated analog-to-digital converters (ADCs), leads to a significant increase in power consumption [4], which is a critical bottleneck for future sustainable optical networks. Although analog circuits are affected by noise, mismatch, and PVT variations, neural network-based approaches can tolerate these non-idealities [5], enabling computation directly in the analog domain without repeated data conversion. In this context, analog AI accelerators are a promising alternative for energy-efficient inference [6].

Here, we propose an ultra-high-speed four-quadrant transconductance multiplier in 22 nm FD-SOI CMOS technology [7] as a core building block for high-speed analog AI accelerators targeting optical link equalization. The circuit exploits the back-gate modulation capability of FD-SOI to perform highly linear signed multiplication. The multiplier consists of two differential pairs sharing a common tail current source, where the differential input voltage is applied to the gate terminals and the differential weight voltage to the back-gates. The weight voltage controls the total current of each pair, while the input signal redistributes the current within each pair. Assuming square-law behavior in strong inversion, the topology operates as a four-quadrant multiplier based on current steering and symmetry, where linearity results from the cancellation of dominant nonlinear terms. As a result, the differential output current is proportional to the product of input and weight and can be described by $I_{\mathrm{od}} = \beta \cdot \gamma \cdot V_{\mathrm{id}} \cdot V_{\mathrm{wd}}$, where β is the transconductance parameter, γ is the sensitivity of the threshold voltage to the back-gate bias, V_{id} and V_{wd} are the differential input and weight voltages, respectively.

Several multipliers can be connected such that weighted summation is naturally performed through Kirchhoff's current law. The summed current can then be integrated on a capacitor, which can be extended toward the implementation of a sigmoid-like activation function, enabling a fully analog neuron. The architecture was verified by simulation with a total bias current of 20 µA at multi-GHz circuit operation. Simulations of a 7-tap analog FIR equalizer further demonstrate PAM4 equalization at 25 GBd for a low-pass plus chromatic-dispersion channel with $D = 17$ ps/nm/km, $\lambda = 1.55$ µm, and fiber length $L = 15$ km. The architecture can be further scaled through time interleaving to increase throughput without proportionally increasing clock frequency, providing a CMOS-compatible path toward low-power analog equalization in future optical interconnects.

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