Portability of RRAM Compact Models across Open-source Circuit Simulators

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Modern neuromorphic systems often rely on Resistive Random-Access Memory (RRAM) devices to accelerate computation through the analog In-Memory Computing (IMC) paradigm [1]. Such trend has been also driven by advances in compact modeling, enabling accurate representation of RRAM behavior in circuit simulations [2, 3]. These models are typically implemented in Verilog-A, allowing seamless integration into SPICE environments while leveraging high-level language constructs. However, they are generally developed and validated using commercial Electronic Design Automation (EDA) tools that fully support the Verilog-A Language Reference Manual, making comprehensive language support a prerequisite for correct model operation. In parallel, open-source chip design flows are rapidly maturing, offering a promising path to reduce costs and broaden access to chip fabrication [4]. This democratization of hardware development is particularly relevant for research-driven and high-risk domains such as the neuromorphic field.

Table 1

	Stanford-PKU RRAM model		Unimore RRAM model		Skywater RRAM model	
	R	P	R	P	R	P
Ngspice-45 w/ OpenVAF	Initialization Issue	✓	Core Dump	Core Dump	Unsupported feature (hidden-state)	Unsupported feature (hidden-state)
Xyce-7.8 w/ ADMS	Unsupported feature (idt)	Unsupported feature (idt)	Behavioral Discrepancy	✓	Behavioral Discrepancy	✓

R = RRAM switched applying voltage **R**amps stimuli (analogous to Quasi-Static measurements)
P = RRAM switched applying voltage **P**ulses stimuli (common procedure in IMC chip)

While significant progress has been made, the adoption of open-source EDA tools for analog IMC is still evolving, particularly due to partial support for Verilog-A features. Moreover, an assessment of RRAM models portability across these tools is missing. In this work, we address this gap by evaluating three established RRAM compact models on two open-source circuit simulators. Simulations are performed on 1T1R structures using NMOS devices from the IHP 130nm open-source PDK [5], with commercial EDA results as reference. For each case study, we compare the simulations results, identify unsupported Verilog-A features, and document the code modifications required for compatibility with each simulator (Table 1). Notably, none of the models were native-compatible with considered tools. This analysis provides practical guidelines for integrating RRAM models into open-source analog design flows, supporting the broader adoption of neuromorphic hardware.

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