Memristor Readout with Current-Based ADC for In-Memory Computing

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In-memory computing is promising to break the von-Neumann bottleneck of conventional computer architectures. Information is stored as transconductance across a memristor based crossbar array, applying a voltage vector as input signal. Reading the output current vector enables e.g. the implementation of a vector-matrix multiplication (VMM) process [1][2].

In this report, we propose the peripheral circuits required for electroforming, set, reset, and readout of the memristor with a current reuse circuitry for minimum power consumption shown in Fig. 1(a). The circuits are part of a system on chip realized later this year as a demonstrator for multiple use neuromorphic computing paradigms within the NEUROTEC II project, funded be the BMBF. It will consist of several computing arrays using the current reuse readout to allow for a flexible use of the implemented crossbar arrays, consisting of co-integrated memristors [3].

A voltage regulator is used to generate the input voltage for the crossbar array to reduce the complexity and requirements of the DAC. To read the current from the memristor, we propose an interface circuit using a PMOS in a cascode structure to work as a single-transistor regulator providing a second reference voltage to the memristor. Then, to reuse the current from the memristor, a current-mode ADC is implemented. The crossbar is implemented using a 3.3 V I/O CMOS devices for electroforming, set, and reset mode. Thanks to the read interface, it is possible to implement the ADC using core CMOS devices with a 0.9 V power supply. This will lead to smaller, lower-power, and faster data conversion performance. Furthermore, it will also allow the ADC to run with or without a transimpedance amplifier for a low power mode. To proof the principle of work of the circuitry this test chip was designed. The voltage regulator, the read interface, and the ADC is implemented for a tape out using 28 nm CMOS technology. The measurement result of the ADC gain tuning and read interface is shown in Fig. 1(b), while the measurement result of the ADC is shown in Fig. 1(c). The presentation will compare the achieved results with state of the art crossbar readouts.

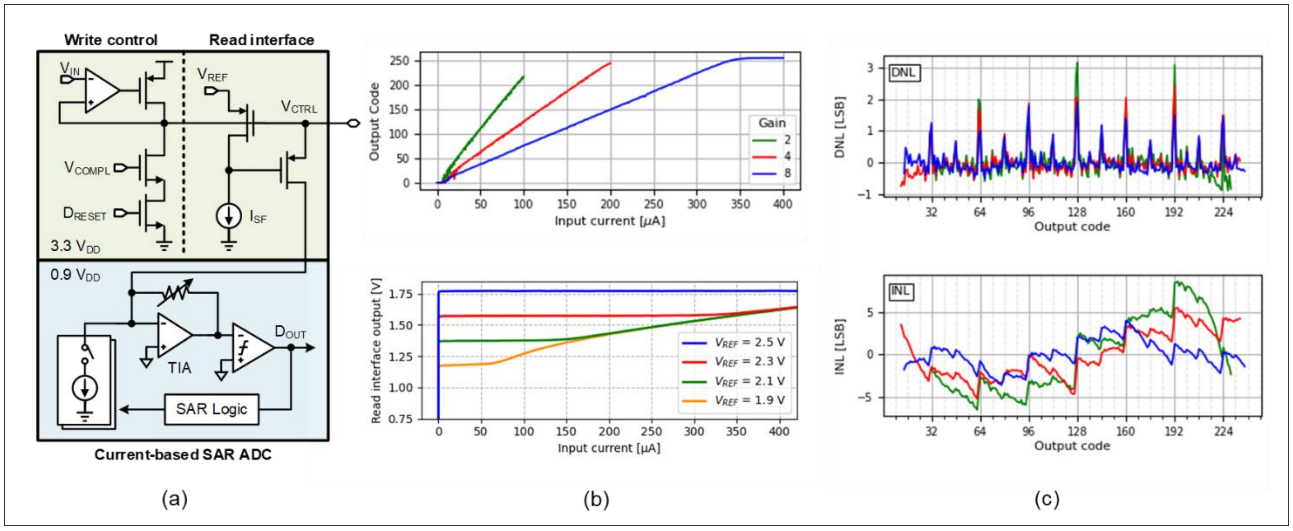

Figure 1. (a) Proposed memristive crossbar-array periphery circuits implemented using 3.3V and 0.9V CMOS devices (b) ADC gain tuning and read interface measurement results (c) ADC measurement results

[1] A. Mehonic et al., Advanced Intelligent Systems, 2.11 (2020): 2000085
[2] F. Cai, et al. Nat. Electron. 2, 290–299 (2019)
[3] Grewing, C. et al. ICNCE (2024)