Fully On-Chip Bio-Plausible Learning and Inference for Memristive Neuromorphic Systems

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Most memristor-based neuromorphic systems focus on inference, relying on energy-intensive offline training [1]. In contrast, the biological brain co-integrates learning within its physical architecture, enabling efficient, continual adaptation at the edge. Predictive coding (PC) suggests that the brain minimizes errors between internal predictive models and sensory inputs [2]. Furthermore, PC occurs at the cellular level within cortical pyramidal neurons (Figure 1(a)). These neurons receive learning signals through their apical dendrites, which then modulate basal synapses to correct network-wide prediction errors [3].

In this work, we present the simulation of a standalone memristive-based circuit that realizes PC-based on-chip learning and inference, see Figure 1(b). We exploit the analogy between biological synaptic potentiation and the voltage-dependent conductance changes in filament-based memristors. Our system utilizes a 2-2-1 neural network in which memristors serve as synaptic weights and learning signals S_L are delivered through the non-inverting inputs of operational amplifiers. A feedback loop compares the output signal S_{out} to a reference S_{ref} (the prediction model) using a control system. The resulting learning signal S_L adjusts neuronal activity until the network converges to the desired response. We demonstrate that this circuit autonomously learns the XOR operation without external software intervention (Figure 1(c)). This architecture provides a scalable path for integrating bio-plausible learning directly into memristive hardware.

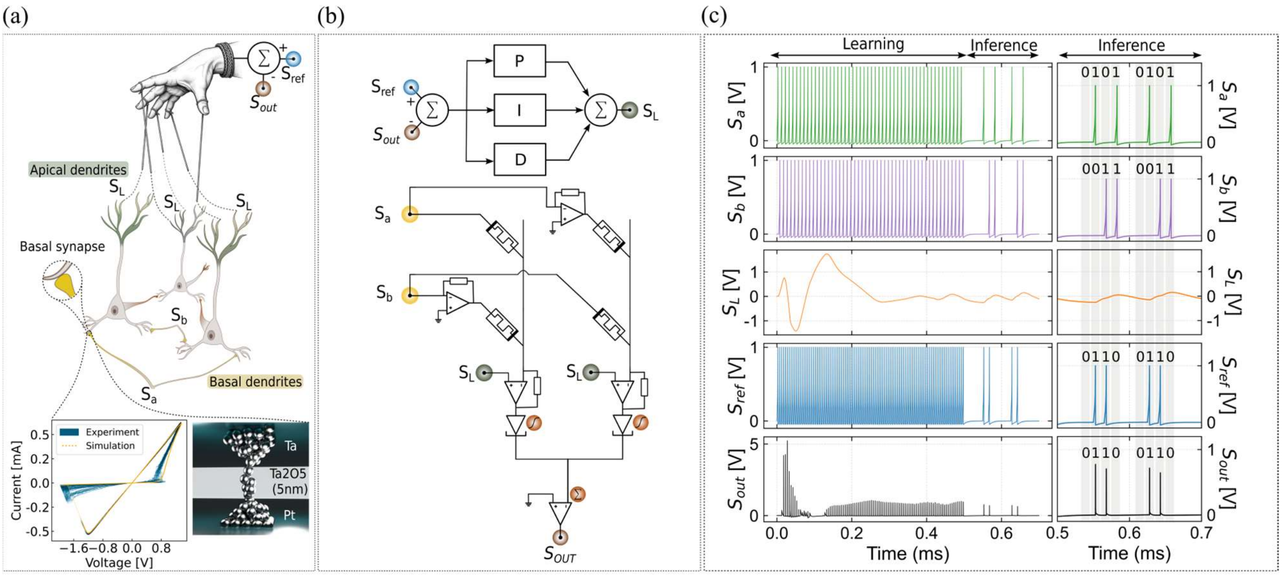

Figure 1: PC-based neuromorphic architecture and hardware implementation. (a) Conceptual framework illustrating distal control signals modulating basal synaptic plasticity via apical dendrites (represented by the puppeteer's hand). Basal synapses are implemented using Ta_2O_5-based memristive devices, with bottom panels showing the alignment between experimental data and custom model simulations. (b) Circuit schematic of the PC-based neural network featuring a single hidden layer. (c) Simulation results demonstrating autonomous adaptation for XOR logic operation.

[1] Aguirre, F., et al. *Nat Commun* **15**, 1974, 2024.
[2] Bastos A. M., et al., *Neuron* **76** 695–711, 2012.
[3] Aceituno P. V., et al., *bioRxiv* 2024.04.10.588837, 2025.