

Fully-analog low-power spike-based processing pipeline for IoT sensory nodes

G. Leo⁽¹⁾ X. Zeng⁽²⁾ N. Burgler⁽¹⁾ N. Garg⁽¹⁾ G. Brandsteert⁽²⁾ T. Ratier⁽²⁾ D. Flandre⁽²⁾ and E. Chicca⁽¹⁾

⁽¹⁾ BICS, Zernike Institute for Advanced Materials and Groningen Cognitive Systems and Materials Center (CogniGron), University of Groningen, The Netherlands ⁽²⁾ ICTEAM, UCLouvain, Belgium

Conventional signal processing pipelines consume significant power due to their reliance on high-frequency sampling and analog to digital converters. To advance low-power Internet of Things (IoT) sensory nodes, we propose a spike-based processing pipeline (see Fig. 1) that performs signal processing directly in the analog domain.

The proposed system utilizes novel artificial spiking sensors based on vanadium dioxide (VO₂) memristors, which generate self-oscillating analog signals to encode temperature (30 - 50 °C) [1] and pressure (0 - 100 kPa) [2] stimuli into spike trains. Each sensor's output is scaled in amplitude and frequency by an analog conditioning circuit before being fed to a downstream processing stage consisting of a compact Spiking Neural Network (SNN). Feature extraction is performed by a bank of N_{S_x} Resonate-and-Fire (R&F) neurons [3] per sensor modality S_x acting as frequency-selective filters tuned to specific temperature or pressure ranges. The signal is then passed to a layer of $N_{S_1} \times N_{S_2}$ Time Difference Encoder (TDE) neurons [4,5]. Each receives input from pairs of R&F neurons and performs multimodal integration through coincidence detection, encoding temporal correlations between different sensory modalities. Classification is performed by an output layer of N_C Leaky Integrate-and-Fire (LIF) neurons corresponding to the number of output classes C . A Winner-Takes-All (WTA) mechanism guarantees the selection of a single class. We validated the feasibility of real-time classification by testing the individual components of the temperature-pressure detection pipeline.

The building blocks of the proposed pipeline are hardware-validated neuromorphic circuits with low power consumption. The architecture is designed for a limited set of discrete classes (e.g., $C = 3$, as shown in Fig. 1). This design choice aligns with real-time hazard detection in monitoring applications, where the primary requirements are low latency and continuous operation rather than high-resolution sensing. The proposed analog system aims for always-on operation and low-power consumption, making it a promising solution for energy-constrained scalable sensing platforms.

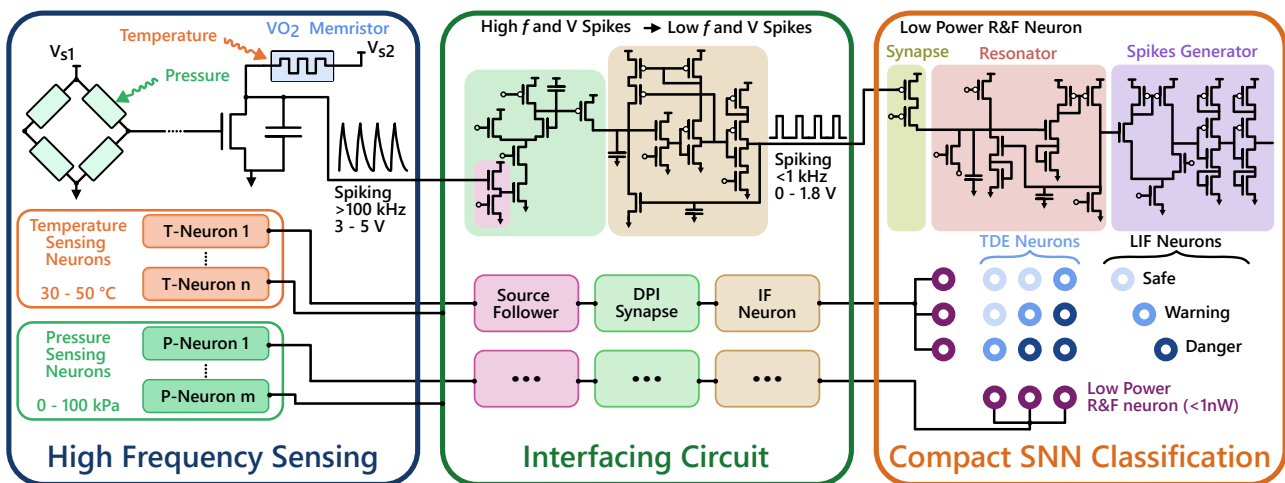


Figure 1: Proposed fully analog spiking pipeline from sensors to SNN.

[1] X. Zeng et al., Phys. Rev. Appl., 2026 (Under review) [2] X. Zeng et al., 2026 (In preparation) [3] G. Leo et al., 2026 IEEE International Symposium on Circuits and Systems, 2026 (In press) [4] M. Milde et al., Neural Comput., 30(9), 2384-2417, 2018 [5] T. Schoepe et al., Nat. Commun., 15(1), 817, 2024