An Asynchronous Switched Ferroelectric Non-Volatile Capacitor Neuron

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Ferroelectric non-volatile capacitors (nvCaps) [1] are a variation of ferroelectric capacitors that make use of the hysteretic, non-volatile capacitance of ferroelectric capacitors. The memory state is encoded in the polarization of the ferroelectric layer, which leads to a change of the device capacitance. This leads to a programmable capacitance that can be used both for conventional non-volatile memory (NVM) applications, as well as an embedded memory cell. In particular for FeFET-based nvCaps, the small process integration overhead enables the integration of these programmable capacitors directly into analog, mixed-signal or digital circuits with little layout restrictions. Accordingly, the memory devices can be placed directly inside the circuits instead of into separate, large arrays, which minimized area overhead and parasitics.

In this work, building on an existing 28 nm neuron implementation [2], we present a switched-capacitor neuron circuit that uses nvCaps to store synaptic weights and membrane potentials. Integrator circuits using the switched-capacitor method are an efficient implementation of analog integration that offers high reliability, scalability and tunability through their clock-based, time-stepped approach. In our implementation, the programmable nvCap capacitance allows us to change the capacitance of the input capacitors directly, efficiently realizing analog synaptic weights with no additional requirement for capacitor banks, SRAM or non-volatile memory. Due to the high integrability of the FeFETs, here used in a MOSCap configuration to realize nvCaps, these non-volatile capacitors can be integrated directly with the circuits and do not require to be accessed across the chip from a memory array. Further, this implementation potentially reduces the area consumption per synapse by replacing the SRAM synaptic weights with the nvCap that is used both as an analog non-volatile memory to store the synaptic weight, as well as a switched capacitor within the integrator circuit.

In addition, the use of an nvCap as a membrane capacitor enables to switch the neuron between two integration modes: By programming the nvCap, the capacitor can be switched to operate in depletion, weak inversion or strong inversion via the threshold voltage shift. This leads to a linear or non-linear capacitor and thus linear or non-linear integration of the neuron's inputs. Further, the neuron has purely digital inputs and outputs that are following conventional asynchronous protocols which allows integration into large, asynchronous digital systems. Together, this enables high scalability when integrated into event-based neuromorphic systems.
In this submission, we will present simulation results of the designed circuit, based on a commercial 28 nm CMOS PDK, complemented by a physics-based FeFET compact model based on existing FeCap [3] and nvCap [4] compact models.

Overall, this leads to a mixed-signal neuron circuit that allows high synaptic density, in particular in the 28 nm CMOS process used and high tunability due to the analog capability of the ferroelectric memory.

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