

# Optimizing Contact Resistance in 2D Material-based Transistors

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Neuromorphic computing applications could benefit from memristors circuits with two-dimensional (2D) materials [1]. High-performance 2D transistors are required as switching elements to control such memristors in CMOS-integrated arrays. In recent years, significant progress has been made in transistors based on 2D semiconductors, particularly atomically thin transition metal dichalcogenides (TMDs). This progress has been enabled by advances in channel engineering, contact formation, gate-stack design, and integration technologies [2].

Besides these developments, several challenges still remained. One of the most critical issues is the formation of low-resistance contacts for TMDs transistors. In the real device, large contact resistance often arises at the metal-semiconductor interface because of Schottky barrier formation and Fermi-level pinning, which arising from metal-induced gap states (MIGS), defects induced gap state (DIGS) and processing conditions [3]. Since high contact resistance reduces the drive current and increases power consumption, searching for suitable contact materials and deposition conditions is essential for achieving high-performance devices. Compared with conventional metals such as Ni, Pt, Au, Ag, semimetals such as Sb and Bi can saturate the metal-induced gap states, thereby reduce this Fermi level pinning and enable equally low contact resistance on Molybdenum Disulfide (MoS<sub>2</sub>) FETs [4] [5]. As a result, high-quality ohmic contacts can be achieved, as confirmed by both DFT calculation as well as in experimental studies [6].

The TRR404 project A06 aims to reduce the contact resistance in 2D material-based transistors, thereby enhancing the device performances and lowering the power consumption. Different contact metals to MoS<sub>2</sub>, improved the fabrication processes to reduce PMMA residue introduced during the transfer process, for example by employing H<sub>2</sub> plasma cleaning [7], will be investigated. This research is expected to provide a new approach for optimizing the fabrication and performance of 2D devices, while also offering valuable guidance for the development of 2D-material-based one-transistor-one-memristor (1T1M) integrated circuit arrays.

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