Si/SiGe Quantum Well Transistor Emulating Biological Synaptic Plasticity for Energy-Efficient Neuromorphic Computing

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As artificial intelligence continues to scale, the energy gap between conventional von Neumann hardware and biological neural systems has become one of the most pressing challenges in modern computing. Si/SiGe quantum well (QW) transistor with a vertical architecture was reported as an artificial synapse using TCAD simulations [1] and as cryogenic electron-based flash memory [2]. In this work, we experimentally demonstrate a planar Si/$Si_{0.8}Ge_{0.2}$/Si QW Schottky barrier MOSFET (SB-MOSFET) as an artificial synapse. The valence-band offset of 148 meV at the Si/SiGe interface forms a buried QW, enabling controlled hole trapping and de-trapping for programmable conductance modulation. A positive gate bias drives hole accumulation into the QW raising channel conductance during reading, while a negative gate bias depletes trapped holes, yielding a nonvolatile and tunable synaptic weight state.

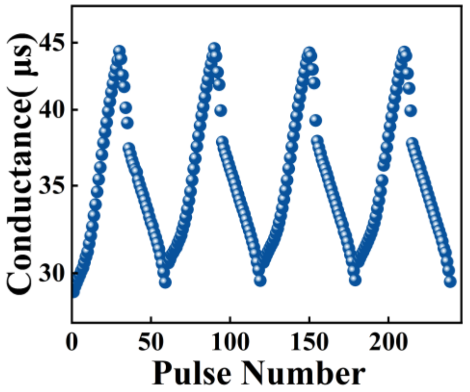

Figure 1: Long-term potentiation/depression of the synapse by measuring the conductance of the transistor as a function of pulse number, demonstrating good linearity, high symmetry and very small cycle-to-cycle variation.

A heterostructure comprising a 15 nm slightly phosphorous doped Si cap, a 20 nm boron-doped $Si_{0.8}Ge_{0.2}$ layer (~10^{17} cm^{-3}) was grown by reduced pressure CVD on a Si substrate, using H_2-SiH_4 and H_2-SiH_4-GeH_4 gas mixtures, respectively. The device was fabricated with a CMOS process using HfO_2 as gate dielectric and nickel disilicide ($NiSi_2$) as source and drain Schottky contacts. We demonstrate that a single transistor can be operated as a short-term memory by writing with a high gate voltage .The memory shows retention time of one hour at room temperature and a high endurance. The device also characterized as an artificial synapse. The short-term plasticity and long-term plasticity are successfully emulated through constant-amplitude and stepwise increasing gate voltage pulse schemes. The measured potentiation and depression as shown in Fig.1 indicate good linearity and symmetry, as well as low cycle-to-cycle variation. The device shows high-energy efficiency with a low energy consumption of 0.8 pJ/spike, confirming Si/SiGe QW SB-MOSFETs as viable CMOS building blocks for energy-efficient neuromorphic hardware.

[1] S. Y. Woo et al., *IEEE Trans. Electron Devices*, 67(9), 3832–3838, 2020.

[2] W. C. Hou et al., *ACS Appl. Electron. Mater*, 4(6), 2879–2884, 2022