Variability-Aware In-Memory Computation in 1T1R RRAM Arrays

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Neuromorphic and in-memory computing (IMC) paradigms address the von Neumann bottleneck by co-locating computation with data storage, reducing costly data movement between memory and processing units [1]. Logic-in-memory (LiM) represents an attractive IMC subset, enabling Boolean logic operations to be executed directly within memory arrays [2]. Among LiM approaches, stateful logic, where both inputs and outputs are encoded as resistive states, is especially well suited for cascaded logic and arithmetic operations relevant to machine learning, cryptography, and signal processing. Resistive random-access memory (RRAM) is a leading candidate for stateful LiM owing to its non-volatility, CMOS compatibility, and ability to represent logic states through distinct resistance levels [3]. However, stochastic variations in RRAM switching parameters introduce intrinsic cycle-to-cycle (C2C) and device-to-device (D2D) variability that directly impacts logic correctness. Despite being well documented at the device level, the propagation of this variability to logic-level reliability remains insufficiently understood, limiting the practical deployment of RRAM-based stateful logic in neuromorphic computing systems. In this work, we address this gap through a combined experimental and analytical investigation of device variability in a 180 nm CMOS-integrated TaO_x/Ta 1T1R RRAM crossbar array. We experimentally demonstrate a reconfigurable MAGIC-based functionally complete Boolean logic set and validate in-memory arithmetic through a half-adder implementation. Through extensive statistical characterization of 1T1R RRAM devices, combined with analytical MAGIC logic gate models and variability-aware Monte Carlo simulations, we identify the dominant variability source driving logic failures. We then derive explicit device-level specifications that are needed for error-free stateful LiM operations. These results provide actionable co-design guidelines bridging device physics and logic architecture for robust, energy-efficient neuromorphic and reconfigurable computing systems.

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