Analysis of BEOL TiO_x memristor variability for neuromorphic applications

D. Florini[(1,2)], N. Garg[(1,2,3)], E. Muhr[(4)], S. Nizar[(1)], J.-M. Portal[(4)], S. Ecoffey[(1,2)], F. Alibart[(1,2,3)], and D. Drouin[(1,2)]

[(1)]Institut Interdisciplinaire d'Innovation Technologique (3IT), Université de Sherbrooke, Sherbrooke, QC, Canada, [(2)]Laboratoire Nanotechnologies Nanosystèmes (LN2) – IRL 3463, CNRS, Université de Sherbrooke, Sherbrooke, Canada, [(3)]Institute of Electronics, Microelectronics and Nanotechnology (IEMN), Université de Lille, Villeneuve-d'Ascq, France, [(4)]Aix Marseille Univ, Université de Toulon, CNRS, IM2NP, Marseille, France

Memristive devices are potential candidates for the hardware implementation of synapses in spiking neural networks (SNNs). Their appeal lies in their dual capacity of weight and plasticity implementation, coupled with the feasibility of monolithic integration in the back-end-of-the-line (BEOL) of conventional CMOS integrated circuits. Despite significant progress in standalone device characterization, BEOL-integrated memristors for SNN applications remain underdeveloped. In particular, TiO_x-based 1T1R architectures—despite the early prominence of TiO_x in the field—suffer from a lack of reported BEOL array-level statistics. This scarcity of empirical data forces many neuromorphic simulations to rely on heuristic estimation of device variability, limiting their predictive accuracy.

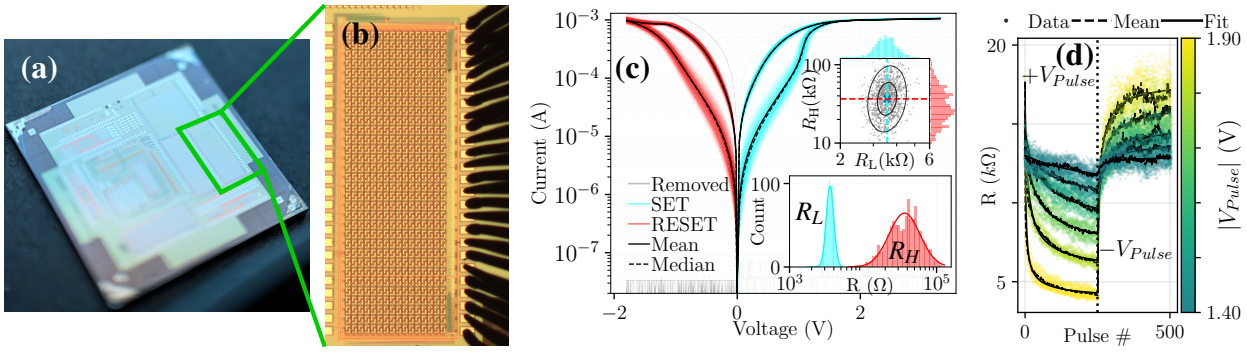

Figure 1: (a) Photo of the UNICO chip. (b) The 32x32 1T1R memristor array during the electrical characterization. (c) I/V cycles of the 1024 devices and relative statistics. (d) Potentiation and depression experiment of a device at different pulse voltages.

We report the characterization of a 32×32 1T1R serially-accessed array, which demonstrate the monolithic integration and functional co-operation of BEOL TiO_x memristors with a commercial 130 nm CMOS chip (UNICO). The UNICO chip (Fig. 1a) is a custom designed and commercially fabricated CMOS chip for analog SNN demonstration [1]. The TiO_x memristive devices are in-house fabricated employing a thermal budget and materials compatible with BEOL processing [2]. The array exhibit a 99.1% DC sweep yield, with only 8 open circuits and 1 short among the 1024 devices. Measured at 0.2V, both high- (R_H) and low- (R_L) resistance states conform to log-normal distributions (Fig. 1(c)). Device performance in the pulsed regime is characterized using multiple repetition of 200 ns pulse trains of varying amplitudes (Fig. 1(d)). By fitting the average potentiation and depression curves, we extract device-to-device (D2D) variability in programming linearity and resistance range. Cycle-to-cycle (C2C) variability is estimated using the RMS difference between the fits and the experimental data. The resulting distributions allow for hardware-realistic C2C and D2D variability to be integrated into neuromorphic simulation frameworks.

[1] N. Garg, PhD thesis, Université de Lille; Université de Sherbrooke (Québec, Canada), 2024

[2] A. El Mesoudy et al., Microelectron. Eng., 255, 111706, 2022.