Development of ion-beam deposition and etching processes for 3D integration of phase-change memory materials in arrays

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Phase-change memory (PCM) has been successfully demonstrated for non-volatile data-storage and memory applications through reversible switching between amorphous and crystalline states [1]. Future computing architectures would benefit from integration schemes that combine PCM with circuit elements to realize a higher integration density in a back-end-of-line (BEOL) compatible, compact 3D layout (Figure 1A). In this work, a system capable of dual ion beam deposition (IBD) and etching (IBE) (Coat 200, scia Systems GmbH, Germany) was utilized for these process developments on a wafer scale.

Films realized by IBD can benefit from the high surface mobility of condensing particles, leading to smooth films with additional densification by an assisted ion beam source. TiN_x was firstly investigated as a bottom-electrode material by reactive deposition using a Ti target and an N_2-assisted ion beam source. The films deposited under conditions of 25 sccm Ar and 20 sccm N_2 exhibited a smooth surface with an RMS roughness of 0.373 ± 0.028 nm (Figure 1B) while maintaining a low resistivity of 109.6 ± 2.3 μΩ·cm, suggesting its potential as a bottom-electrode layer for further integration. The IBE protocols were established using directional Ar^+ physical etching for patterning complex structures. For the TiN_x bottom-electrode layer, a beam voltage of 400 V, an accelerator voltage of 200 V, and a beam current of 400 mA with 30 sccm Ar were used, giving an etch rate of approximately 0.125 nm/s with an assisted end-point detection. For patterning the PCM layer, a lower-energy recipe was used with a beam voltage of 200 V, an accelerator voltage of 450 V, a beam current of 280 mA, and 30 sccm Ar. As an example, a 25 nm $Ge_2Sb_2Te_5$/5 nm $(ZnS)_{80}$:$(SiO_2)_{20}$ stack (previously deposited in another sputtering instrument) showed a controllable etch rate of around 0.55 nm/s (Figure 1C). Because of using a chemically inert gas, this physical etching approach is expected to reduce chemically induced composition changes compared with reactive etching processes [2]. The results suggest a relatively uniform etched surface without obvious large-scale roughening or severe surface damage (Figure 1D), supporting its compatibility with subsequent multilayer device fabrication. Our next step is to develop a complete process flow for fabricating PCM crossbar arrays and to evaluate switching and array performance, including SET/RESET behavior, resistance contrast, access time, and cyclic endurance.

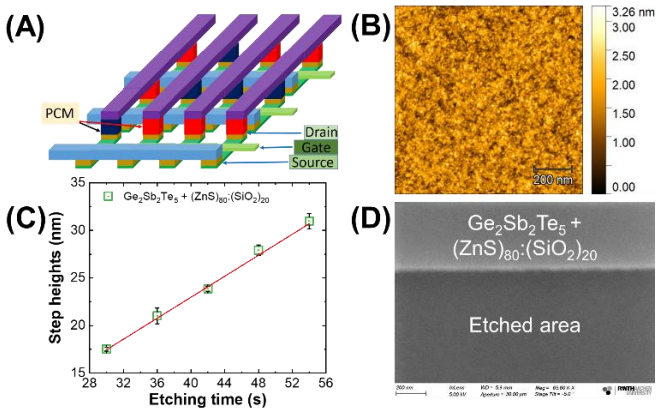

Figure 1: (A) Conceptual 1T1R PCM array integration scheme. (B) AFM image of TiN_x thin film used as the bottom electrode. (C) Etch-depth-versus-time plot for the PCM stack. (D) SEM image of the etched PCM stack.

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[2] J. Li *et al.*, *Appl. Surf. Sci.*, vol. 378, pp. 163–166, Aug. 2016.