Network Size Optimization and Visualization of Reservoir Node Contributions Using the Backward Method for Graphene Electric Double-Layer Transistor-Based Physical Reservoir Computing

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In recent years, the rapid advancement of AI technologies and the expansion of their applications and users have led to increasing concerns regarding computational latency and power consumption caused by the enormous computational cost of AI processing[1]. To address these issues, physical reservoir computing (PRC) has attracted considerable attention as an energy-efficient computing paradigm. Unlike conventional multilayer neural networks, PRC consists of only three layers: an input, a reservoir layer, and an output layer. Leaning is performed by utilizing nonlinear physical responses in the reservoir layer. The reservoir is required to possess nonlinearity, short-term memory, and high dimensionality; however, it remains unclear which device characteristics predominantly contribute to computational performance. In this study, we investigated which parameters contribute to computational performance by combining the NARMA2 benchmark task with the backward method while maintaining computational performance[2,3]. The backward method is a node selection technique used to identify computationally important reservoir nodes by sequential node removal while evaluating performance using the NARMA2 benchmark task. For the PRC implementation, we employed an ion-gating reservoir (IGR) based on an electric double-layer transistor (EDLT). The device show in Fig. 1(a) is an EDLT employing monolayer graphene as the channel material. By applying a gate voltage (V_G), the transistor exhibits a V-shaped current-voltage (I-V) characteristic, as shown in Fig. 1(b). This nonlinear characteristic was utilized as the reservoir layer, and the resulting current responses were used as reservoir states for computation. By applying the backward method to 140 reservoir states, we successfully identified the node positions contributing to computational performance while preserving the overall computational accuracy, as shown in Fig. 1(c). The results revealed that nodes exhibiting short-term memory effects and nodes corresponding to changes in the applied V_G significantly contributed to computational performance. Computational performance was maintained with an NMSE of 0.0152 after reducing the reservoir nodes from 140 to 70. These findings provide insights into the design of high-performance next-generation AI devices and contribute toward their practical implementation.

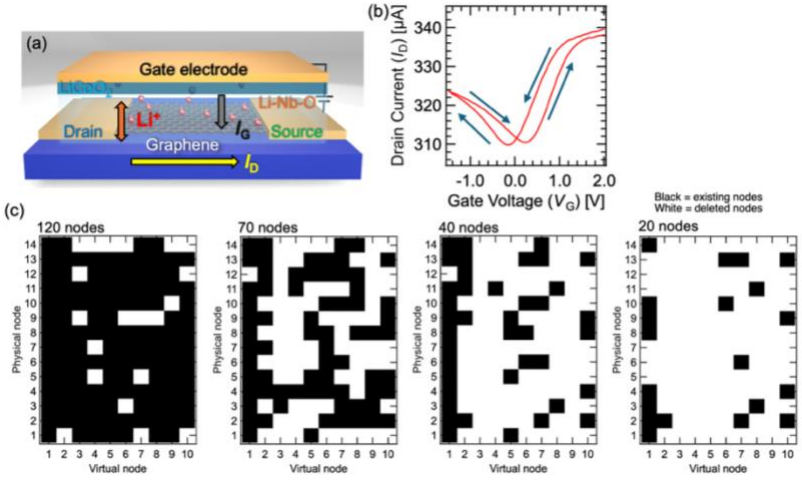

Figure 1: (a)The schematic of graphene EDLT device[2,3],
(b) The V shaped I-V characteristic, (c) Results of the backward method[3]

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