Analog Feed-Forward Neuron: Breadboard Implementation and Training Dynamics for Binary Pattern Classification

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Abstract — Analog neural networks offer compelling advantages for edge AI: ultra-low power, parallel computation, and continuous-time dynamics. This work presents a complete breadboard implementation and experimental characterization of a single analog feed-forward neuron (Clarke's architecture) using LM324N op-amps, AD633ANZ four-quadrant multipliers, and 1 µF ceramic capacitors for synaptic weight storage. Real-time delta-rule learning is demonstrated with full oscilloscope visualization of convergence.

The circuit implements four functional blocks: capacitive weight storage, weighted summation via analog multiplication, diode-resistor nonlinear activation approximating tanh(z), and a weight update mechanism realizing $\Delta w_i = \alpha \varepsilon x_i$. An additional AD633 per synapse computes the error-input product; a 2N7000 MOSFET integrates this onto the storage capacitor. The total component cost is under USD 100.

The neuron was trained and tested across four conditions spanning 1 Hz–2.3 kHz and 2–5 V peak-to-peak square-wave inputs. Error signals converged from >1 V to <150 mV within 50–180 ms in all cases. Convergence time decreased with both frequency (180 ms at 1 Hz, 50 ms at 2.3 kHz) and amplitude, consistent with the theoretical A^2 scaling of effective learning rate since both error and input appear multiplicatively in the update rule. Final weight voltages ranged from 112–122 mV (low frequency/amplitude) to 1.36–1.58 V (2.3 kHz/5 Vp-p).

AND and OR gate training achieved 100% binary classification accuracy across all four input patterns, confirmed by post-training logic verification (Table I). XOR training failed to converge as expected for a linearly inseparable function, confirming genuine neural computation. Weight voltage SNR remained >30 dB below 1 kHz, degrading to ~18 dB at 2.3 kHz due to LM324N slew-rate limits; capacitor leakage was 3–10 mV/min, sufficient for demonstrations under 10 minutes. The optimal operating range is 1–2 kHz.

Table I. AND Gate Verification After Training

Input (x_1, x_2)	Target	Measured Output	Correct?
(0, 0)	−1	−1.1 V	Yes
(0, 1)	−1	−0.9 V	Yes
(1, 0)	−1	−0.8 V	Yes
(1, 1)	+1	+1.3 V	Yes

These results validate three key principles: (1) capacitive synaptic storage is practical with zero standby power; (2) the delta rule translates reliably to discrete analog hardware; and (3) oscilloscope observation provides unprecedented visibility into learning dynamics. Run-to-run weight variability was ~13%, attributable to AD633 multiplier tolerances (±1% gain). Future directions include PCB integration, microcontroller-automated training, and scaling to a two-layer topology for linearly inseparable classification tasks.

References

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